V6065

3U VPX Versal® Premium ASoC FPGA Optical I/O Module with XMC Site

Benefits

Heterogeneous computing card combining hard ARM processor cores, large FPGA fabric, and high-bandwidth interfaces

Designed specifically for sensor interface, digital signal processing, video processing, application co-processing, and secure networking

HPEC focus, 3U VPX, VITA 42 XMC compliance, VITA 47 compliance and SOSA aligned options

Versatile design supports electrical or optical interfaces, optical options for both backplane or front-panel I/O

Modular optics for flexibility in supporting 1-25G per lane

Features

Xilinx® Versal® ASoC (FPGA): VP1502/VP1702

Up to twelve (12) 1G to 25G optical ports via MPO front panel I/O or VITA 66 optical backplane I/O

PCIe Gen3/Gen4 support

Thermal sensors for monitoring card temperature

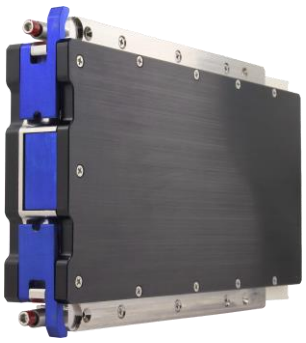
Robust FPGA example design

3 banks of 16GB (48GB total) up to 1866MHz / 3733 Mbps LPDDR4 SDRAM

Compute-intensive profile with XMC site routing to the Versal® as PCIe or high-speed serial

Petalinux BSP

Hard silicon MACSEC implementation in Versal® ASoC (FPGA) device



Overview

The V6065 is a next generation heterogeneous embedded computing 3U VPX module featuring the Xilinx® Versal® Premium Adaptive System-on-Chip (ASoC), rugged optical and electrical high-speed I/O, XMC site, and SOSA aligned profile options. The V6065 provides options for Versal® Premium VP1502 or VP1702 part selection. In a single 3U VPX card, the V6065 provides three 100G optical interfaces (300G aggregate), large FPGA fabric, ARM processor cores, and XMC site.

The V6065 excels at high-bandwidth interface applications where data is processed or pre-processed locally and then distributed across the VPX backplane or optical interfaces. Use cases include sensor interface, data processing, data distribution, and FPGA co-processing applications. Radar, signals intelligence, electronic warfare, video, storage, medical imaging, and embedded communications systems all can benefit from the V6065 module.

By leveraging the Versal® hard silicon Ethernet interfaces, PCIe controllers, DMA engines, and associated software drivers Xilinx® has enabled a robust ecosystem for high-bandwidth Ethernet performance. In addition to the Ethernet interface, the FPGA fabric provided within the ASoC part is capable of hosting New Wave DV IP cores for Fibre Channel, ARINC-818, sFPDP, Aurora, and others. This makes the V6065 an ideal hardware platform for mixed interface protocol needs or protocol bridging applications.

The V6065 serves as a standalone data interface and processing solution in a single 3U VPX module. The V6065 provides twelve (12) full duplex optical ports supporting from 1-25G per lane, FPGA fabric resources, ARM processor cores, and XMC site. The V6065 can also be used adjacent to CPU's and/or GPUs in a 3U VPX system. In this arrangement, the adjacent CPU's/GPUs are unburdened of the data interface overhead and can be dedicated to running high value applications and algorithms with the V6065 feeding them data directly across the backplane.

The inclusion of an XMC site enables customization and flexibility to meet specific application requirements, such as multi-level security or secure boot. Further, this configuration supports scalability and future XMC module upgrades to increase performance or add new functionalities long into the product's life. Such an approach enables new system design avenues such as XMC based CPU's and GPU's hosted on a 3U VPX FPGA card.

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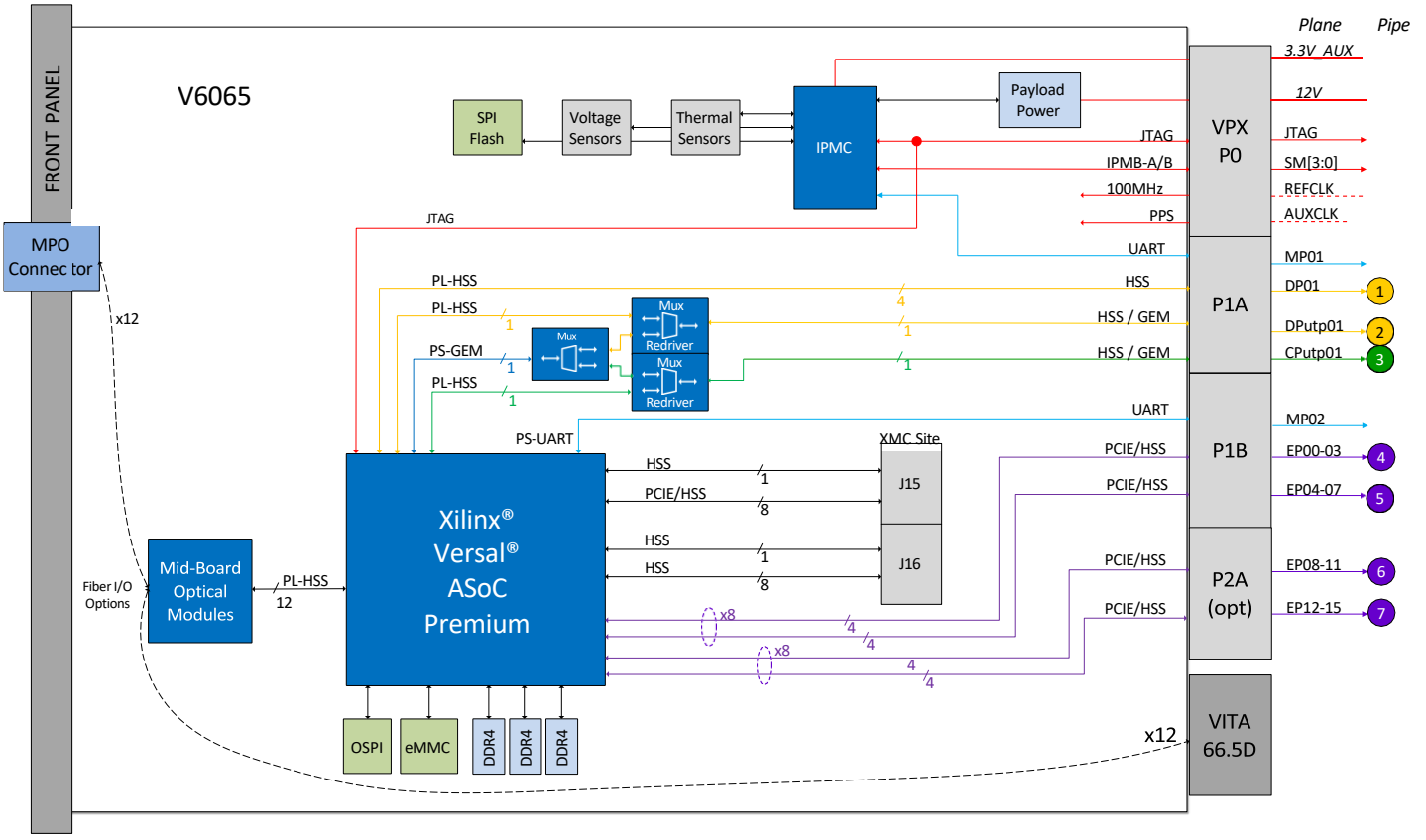


SOSA Plane Legend

CP	Control Plane	EP	Expansion Plane	UP	Utility Plane
DP	Data Plane	MP	Maintenance Plane		

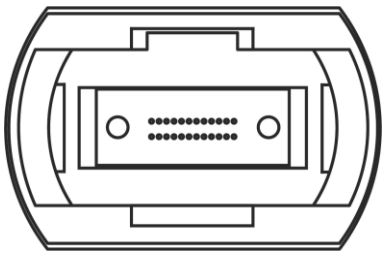
> V6065 Block Diagram

Optical Connector Options

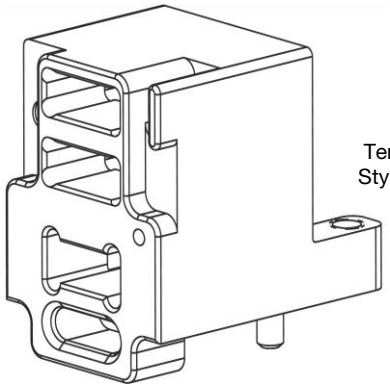
The V6065 offers three different optical I/O options:

1. Optical Front Panel MPO Connector
2. Optical Backplane MT Connector for VITA 66.5
3. No optics

1. Front Panel MPO (Female) I/O



2. VITA 66.5 Backplane MT I/O1



Termination: VITA 66.5 Style D (pictured)

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Multi-Processor Multi-Core Support

The V6065 is uniquely suited for system architectures involving multiple processing cards on a common switched data plane. Specifically, the V6065 supports shared access from multiple host processors, enabling it to function as a cost-effective, high-performance gateway. This feature enables a single high-speed pipe to carry multiple virtual channels in systems that need to spread or load-balance sensor data across processor arrays.

Complete Product Support Program

New Wave prides itself on its excellent customer support, a fact that is echoed by our customers. New Wave DV provides industry standard warranty on its products, but it is the human factor that makes our support so valuable to our customers. Our team takes the time and effort to ensure that the customer experience with our products is a positive one.

Our Commitment

New Wave is committed to providing the latest innovations in technology, architectures, and techniques to keep our customers one step ahead of the rest. Our products, complete with the Development Framework, are intended to offer our customers an entirely unique out-of-the-box experience.

Technical Specifications

NETWORK INTERFACE

Up to twelve (12) 1G to 25G optical ports (front & backplane options)

- 850nm multi-mode optics

22 lanes of electrical high-speed network I/O available to the backplane

OPTIONAL ADDITONAL PROTOCOLS

Ethernet, Fibre Channel, sFPDP, ARINC 818, Aurora

ASoC (FPGA)DEVICE

Xilinx® Versal® VP1502, VP1702

Visit Xilinx® Versal® Datasheet1

MEMORY

3 banks of 16GB (48GB total) up to 1866MHz/3733 Mbps LPDDR4 SDRAM

THERMAL SENSORS

2 digital temperature sensors

COMPLIANCE

VITA 20, 42, 47, 48.2, 65, 66.5

PHYSICAL CHARACTERISTICS

Dimensions:

170.75mm length: Face of carrier to back edge of Guide pin connectors
189.22mm length: MPO flip door to back edge of Guide pin connectors
100mm width: Edge of guide rail to guide rail
24.64mm height: From primary cover to secondary cover

Weight:

<1.764 lbs (800g)

POWER CHARACTERISTICS

Power Draw (Max): 216W
Cooling Capability in 48.2 ECC4 C2 (85° C): 150W
Power Supply: 12V

TEMPERATURE

Operating: -40˚ C to 85˚ C (conduction-cooled)
Storage: -55˚ C to 105˚ C

1Xilinx® Versal® ASoC Datasheet: https://www.xilinx.com/products/silicon-devices/acap/versal.html

V6065 Hardware Part Number Configuration

400	-	06065	-	"WXYZ"	-	"IP"	-	"CC"
Series		Model		Board Configuration		IP Configuration		Coating
				Select 1 for each W, X, Y, and Z		Select 1 IP Option		Optional Select 1 Coating Option

400-06065-WXYZ-IP-CC

W

Config #	Description
2+	*Reserved*
1	Xilinx Versal VP1702 ASoC
0	Xilinx Versal VP1502 ASoC

Y

Config #	Description
0	Conduction cooled, 1" pitch

Z

Config #	Description
3+	*Reserved*
2	Industrial Temp
1	*Reserved*
0	Commercial Temp

IP

Config #	Description
1+	*Reserved*
00	Example design package

CC

Config #	Description
AR	Acrylic conformal coat
UR	Urethane conformal coat
ER	Epoxy conformal coat
SR	Silicone conformal coat
XY	Parylene conformal coat
BLANK	No conformal coat

X

Config #	Slot Profile Description	VITA 65 Compatible Profile	VITA 65 Aperture Style
I+	*Reserved*	*n/a*	*n/a*
H	No optics populated, P2A not populated	14.6.11-0	J*
G	*Reserved*	*n/a*	*n/a*
F	12-lane 1-25Gbps front panel MPO optics, P2A not populated	14.6.11-0	J*
E	*Reserved*	*n/a*	*n/a*
D	12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated	14.6.11-14	J*
C	*Reserved*	*n/a*	*n/a*
B	8-lane 1-25Gbps front panel MPO Optics, P2A not populated	14.6.11-0	J*
A	*Reserved*	*n/a*	*n/a*
9	8-lane 1-25Gbps front panel MPO Optics, P2A not populated	14.6.11-14	J*
8	No optics populated, P2A populated	14.6.13-0	J
7	*Reserved*	*n/a*	*n/a*
6	12-lane 1-25Gbps front panel MPO optics, P2A populated	14.6.13-0	J
5	*Reserved*	*n/a*	*n/a*
4	12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated	14.6.13-8	J
3	*Reserved*	*n/a*	*n/a*
2	8-lane 1-25Gbps front panel MPO Optics, P2A not populated	14.6.13-0	J
1	*Reserved*	*n/a*	*n/a*
0	8-lane 1-backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated	14.6.13-8	J

*14.6.11 Specifies an H style aperture with 2 style C fiber connectors, or an alternative style connector(s) that fit with the aperture space. 14.6.11 options 9, A, D, and E and 14.6.13 options 0, 1, 4 and 5 are delivered with a single style D connector thus meeting the specification of Style H or Style J.

V6065 “Go-Fast” Hardware Part Numbers

Part Numbers from Table 2 are available with the shortest lead times.

Table 2

Config #	Slot Profile Description
“.11” Profiles	
400-06065-1D02-00	V6065 FPGA 3U VPX Module, Xilinx Versal VP1702 ASoC, 12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06065-1H02-00	V6065 FPGA 3U VPX Module, Xilinx Versal VP1702 ASoC, optics not populated, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package

“.13” Profiles	
400-06065-1402-00	V6065 FPGA 3U VPX Module, Xilinx Versal VP1702 ASoC, 12-lane 1-25 Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06065-1802-00	V6065 FPGA 3U VPX Module, Xilinx Versal VP1702 ASoC, optics not populated, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package

FOR MORE INFORMATION
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