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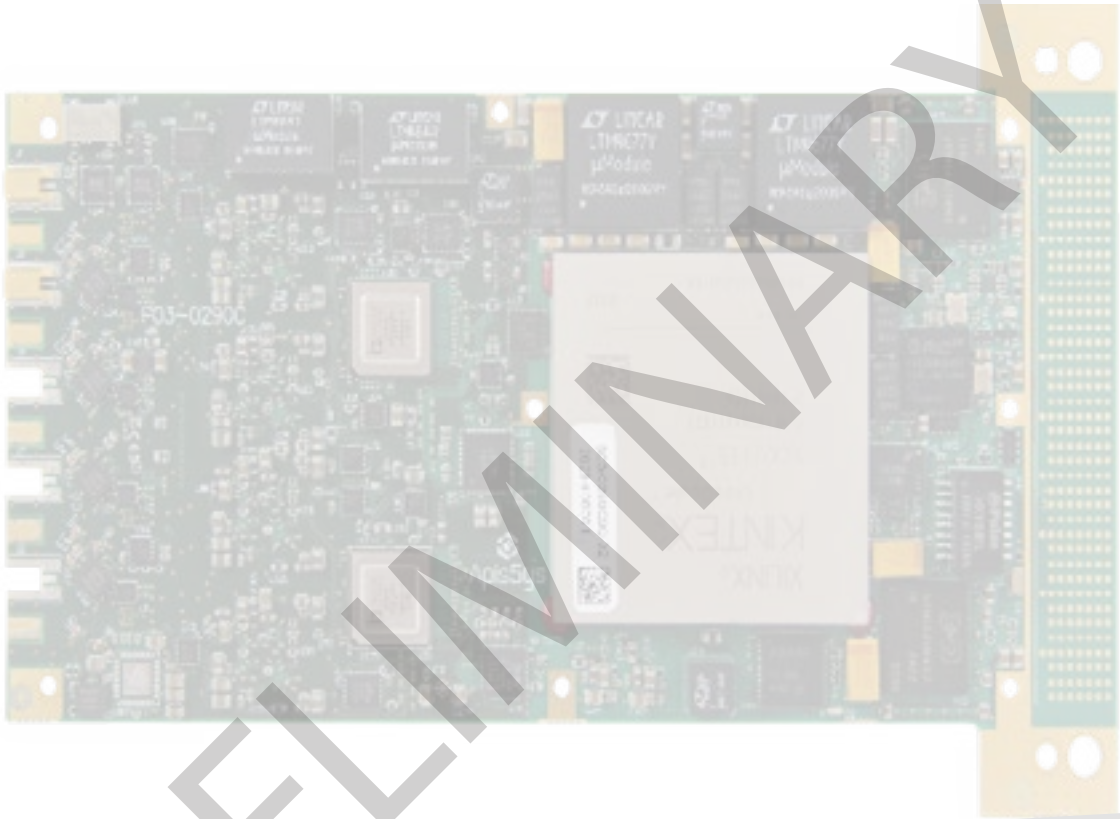
AV 151

Phased-Array Radar Transceiver
EW-ESM/ECM

3U VPX / SOSA
Virtex UltraScale+ FPGA
Quad 12 bit 20 Gsps ADC
Quad 16 bit 28 Gsps DAC
Analog bandwidth up to 18GHz
Conduction or Air-Cooled



Applications

· Phased-Array Radar Transmitter / Receiver
· Electronic Warfare ESM /ECM
· Broadband Communication

Features

. 4 channels 20 Gsps 12-bit ADC
. 4 channels 28 Gsps 16-bit ADC
. Configurable DDC and DUC
. One Ultra Low jitter clock synthesizer
. External or internal sampling clock reference
. User programmable Xilinx® Virtex® Ultrascale+™ VU7P/VU9P/VU13P FPGA
. 2x 64-bit 8GBytes DDR4 2666 SDRAM
. SOSA - aligned
. 48x User-defined IO extension on P2 (optional)

Specifications

Form Factor

- 3U VPX Air-cooled Vita 48.1, pitch 1.0"
- 3U VPX Conduction cooled Vita 48.2, pitch 1.0"

VPX Profile

- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0 (SOSA-aligned)

Analog Inputs/Outputs

- Input coupling: AC
- Full power bandwidth: > 100MHz to 18 GHz
- Full scale : +2 dBm TBD
- Output coupling: AC
- Full power 100MHz to 18 GHz
- Full scale : -4 dBm TBD
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion

- Four channels, up to 20 GHz
- Resolution: 12 bit
- Sampling Performances @20Gsps
  - NSD: -150 dBFS/Hz at -20dBFS at 2GHz
  - HD2/HD3: -65 dBFS at -7dBFS at 2GHz
  - IMD3: -75dBFS at -13dBFS at 2GHz

Digital-Analog Conversion

- Four channels, up to 28Gsps
- Resolution: 16 bits
- Sampling Performances @28Gsps
  - NSD: -164 dBFS/Hz at 0dBFS at 2GHz
  - IMD3: -75dBc at -13dBFS at 2GHz to 10GHz

Virtex Ultrascale+

- XCVU7P-2FLVB2104I
- XCVU9P-2FLGB2104I
- XCVU13P-2FHGB2104I

Data Conversion

- One AD9084 4T4R DF Mixed Signal Front Ends (MxFE)
- 4 ADC Channels 12-bit 20Gsps
- 4 DAC Channels 16-bit 28Gsps
- Analog Bandwidth up to 18GHz
- Configurable DDC and DUC
- Ultra-low jitter clock synthesizer
- External or internal sampling clock reference

Memory

- Two banks 64-bit 8GBytes DDR4 2666 SDRAM
- One 2 Gbit QSPI FLASH memory

Operating Temperature

- Air-cooled EAC6 -40°C to 70°C
- Conduction-cooled ECC3, -40°C to 70°C

Power dissipation (VU13P)

- +12V: 12.4 A max (150W) TBD
- +3.3VAUX: 0.6 A max (2W) TBD

Weight

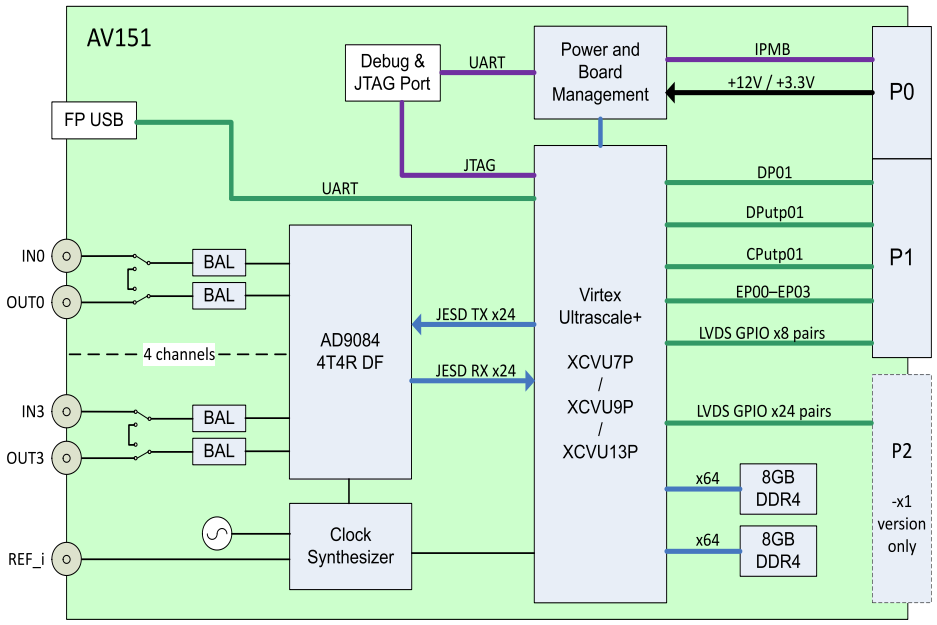
- Air cooled : 550g TBD
- Conduction cooled : 650gTBD

Board Support Package

- FPGA example design
- SW API and examples, Windows 10 64-bits / Linux 64-bits
- User manuals
- Quick start guide

contact: sales@apissys.com

www.apissys.com



VPX interface

- P1:
  - -Data plane: one fat pipe DP01 supporting 40GBASE-KR4, PCIE GEN3 4X
  - -Data plane: one ultra-thin pipe DPutp01 supporting 1000BASE-KX, 10GBASE-KR
  - -Control plane: one ultra-thin pipe CPutp01 supporting 1000BASE-KX, 10GBASE-KR
  - -Expansion plane: one fat-pipe supporting PCIE GEN3 4x / 8x, Aurora
  - -Expansion plane: 8 LVDS differential pairs, configurable as 16 single ended LVCMOS

- P2:
  - -Empty (SOSA-aligned profile)
  - or
  - -24 LVDS differential pairs, configurable as 48 single ended LVCMOS

Environmental	Air-cooled Vita 47 class EAC6	Conduction-cooled Vita 47 class ECC3
Operating Temperature	-40°C to 70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)
Non Operating Temperature	-50°C to +100°C	-50°C to +100°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g²/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.01g²/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing
Operating Attitude	@ -1,500 to 60,000 ft with adequate airflow	@ -1,500 to 60,000 ft

Ordering information

Part	Number	AV151	c	a	b
Cooling	Air	-	A	-	-
	Conduction	-	C	-	-
FPGA	FPGA Virtex Ultrascale+ VU7P	-	-	7	-
	FPGA Virtex Ultrascale+ VU9P	-	-	9	-
	FPGA Virtex Ultrascale+ VU13P	-	-	13	-
VPX P2	Not fitted (SOSA-aligned)	-	-	-	0
	Fitted (48x User-defined IO extension)	-	-	-	1