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high tech
for innovators

AV 127

Wideband communication
Phased Array Radar

3U VPX
Kintex UltraScale FPGA
Up to 1000 Gbps Optical Links interfaces
Conduction or Air-Cooled

apissys

High Speed Data Conversion
& Signal Processing Solutions

AV 127

Applications

· Wideband Communication
· Phased Array Radar
· Electronic Warfare

Features

· 12, 24 or 36 full duplex Fiber interfaces
· Up to 14 Gbps per fiber from 0°C to 55°C (–AS version)
· Up to 10 Gbps per fiber from -40°C to +85°C (-AR, -CA and -CR versions)
· Three independent low jitter clock synthesizers
· User programmable Xilinx® Kintex® UltrascaleTM KU115 FPGA
· 800 MHz 2x 256M64 DDR3 SDRAM
· 3U OpenVPX standard compliant
· Air cooled and Conduction cooled rugged versions

Overview

The AV127 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.
The AV127 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora. The AV127 combines up to 36 full duplex fiber interfaces with ultra-high processing power delivered by Xilinx® Kintex® Ultrascale™ FPGA, making it ideally suited for embedded signal processing applications such as Wideband Communication, Phased Array Radar or Electronic Warfare applications.
The AV127 features three fully independent low jitter clock synthesizers for support of most communication protocols on fiber.
The AV127 includes one Xilinx® Kintex® Ultrascale™ KU115 FPGA for an impressive processing capability of more than 7 TMACs (Multiply Accumulate per second), two high speed 256M64 DDR3 SDRAM memory for data processing and two 1 Gb synchronous FLASH memory for multiple firmware storage.
The AV127 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.
The AV127 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

Optical Links Interfaces

The AV127 supports up to three x12 Optical Links Transmitters and three x12 Optical Links Receivers.
The Optical Links Transmitters and Receivers support up to 14 Gbps on commercial temperature grade (0°C to +55°C) and up to 10 Gbps on industrial temperature grade (-40°C to +85°C).
The Optical links use a proven 850 nm VCSEL array technology.
The AV127 supports three MTP adapters on the front panel supporting x24 MT ferules.

Clock Synthesizers

The AV127 provides one low jitter clock synthesizers for each x12 Optical Links transceiver block.
Each clock synthesizer can synthesize two clock references for the FPGA GTHs from 60 MHz to 820 MHz locked on a common 25 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 14 Gbps.

Memories

The AV127 includes two 800 MHz 256M64 DDR3 SDRAM memory banks and two 1 Gbit QSPI FLASH used to store multiple FPGA configuration files.

FPGA

The AV127 is fitted with a Xilinx® Kintex® Ultrascale™ KU115 user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring sub-system, leaving most of the logic and block RAM and all DSP resources available for customer processing.
Dedicated to signal processing, the Xilinx Kintex Ultrascale KU115 FPGA includes 1,451 K logics cells, 2,160 36 Kbit RAM blocs, 6 PCIe interface blocs and 5,520 DSP48 slices for an impressive processing power of more than 7 TMACs.
The FPGA is delivered in -2 speed grade.

VPX interface

The AV127 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra-Thin Pipes for Control Plane and two User Defined Ultra-Thin Pipes on P1. The AV127 also supports 28 single ended LVCMOS33 plus 8 single ended LVCMOS18 on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.
The AV127 features two low phase noise clock generators able to synthesize clock references for the FPGA GTHs from 60 MHz to 820 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1, 2 and 3, SATA, SRIO and XAUI 10Gbit Ethernet up to 16.375 Gbps.

Microcontroller

The AV127 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision. The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board. The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware

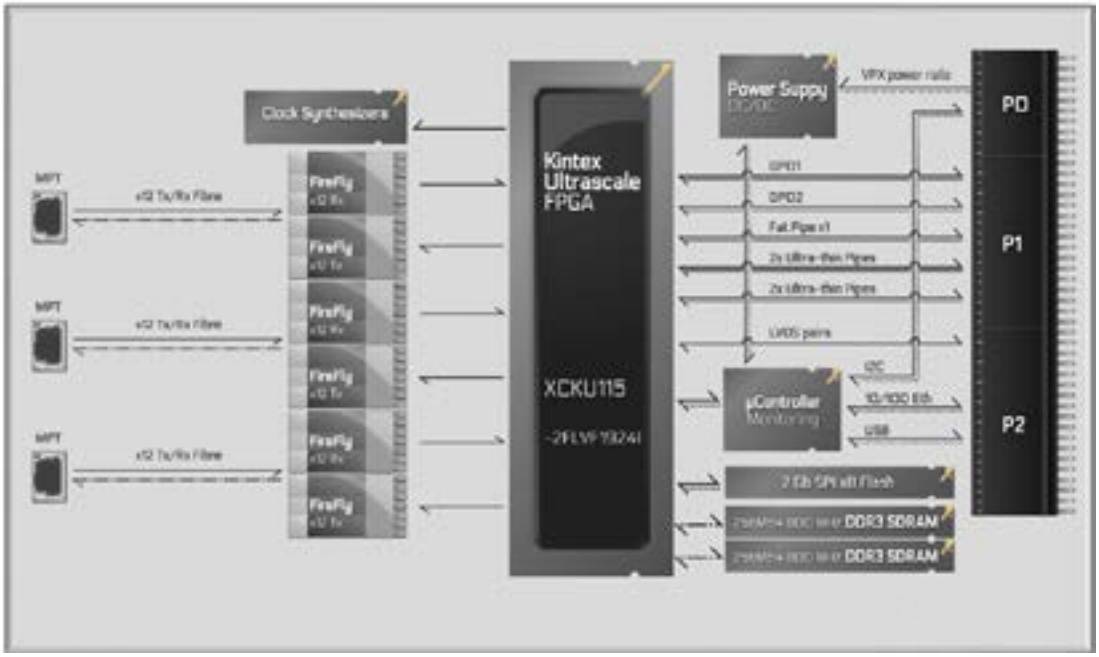
The AV127 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV127 hardware resources.
A base design is provided which demonstrates the use of the AV127 and gives users a starting point for firmware development.
The AV127 firmware package is supported on the Xilinx VIVADO® 2016.2 design suite.

Software

The AV127 is delivered with software drivers for Windows 10 and Linux.

Ruggedization

The AV127 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.



Specifications

Optical Links

- 0, 12, 24 or 36 Optical Transceivers
- 850 nm VCSEL array technology
- 14 Gbps from 0°C to +55°C (-AS)
- Total data throughput up to 1008 Gbps
- 10 Gbps from -40°C to +85°C (-AR, -CS, -CR))
- Total data throughput up to 720 Gbps
- Connectors: MTP adapter

Reference Clocks

- Internal 25 MHz reference or 100 MHz PCIe reference clock
- Three independent clock synthesizers with two clock outputs Frequency: 60 MHz to 820 MHz

FPGA

- FPGA: Xilinx Kintex Ultrascale
- XCKU115-2FLVF1924

Memory

- Two banks 256M64 DDR3 SDRAM, 800 MHz clock
- Two 1 Gbit QSPI FLASH memory

VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 28 single ended LVCMOS33
  - 8 single ended LVCMOS18

Software support

- Software Drivers:
  - Windows 10
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2016.2

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

Power dissipation

- 12V: 6.2 A max (75W)
- +5V: 3.0 A max (15W)
- +3.3V: 3.0 A max (10W)
- +3.3VAUX: 0.6 A max (2.0W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ruggedization levels	AS Air flow, Standard (VITA 47 EAC4)	AR Air flow, Rugged (VITA 47 EAC6)	CS Conduction Standard CS (VITA 47 ECC3)	CR Conduction Rugged (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Attitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 60,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

Ordering information

Part Number		AV127	-	rr	a	b
Ruggedization level	Air Standard		-	AS	-	-
	Air Rugged		-	AR	-	-
	Conduction Standard		-	CS	-	-
	Conduction Rugged		-	CR	-	-
Option 1	FPGA Kintex Ultrascale KU115		-	-	1	-
Option 2	No Optical Links		-	-	-	0
	12 Optical Links		-	-	-	1
	24 Optical Links		-	-	-	2
	36 Optical Links		-	-	-	3

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