New!

Model 3312

4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A - FMC

FlexorReadyFlow Board Support Package

Features

- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Creates a complete radar and software radio interface solution, when combined with the Model 5973 3U OpenVPX Virtex-7 FMC carrier board
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 3312 is a multi-channel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, on-board programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with the Model 5973 3U OpenVPX Virtex-7 Processor and FMC Carrier, the board set becomes a turnkey data acquisition and signal generation solution. For applications that require custom processing, this board set is an ideal IP development and deployment subsystem.

A/D Acquisition Engine

When used with the 5973, the 3312 features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the 5973 for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the 5973's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback Engine

When used with the 5973, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

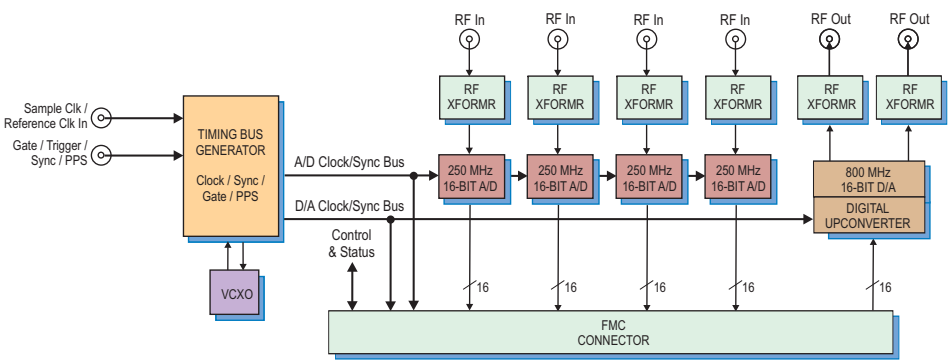
Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converters

The front end accepts four full-scale analog HF or IF inputs at +5 dBm into 50 ohms with transformer coupling into four 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages. ➤



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4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A - FMC

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

FMC Interface

The Model 3312 complies with the VITA 57 FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Full-Scale Input:** 5 dBm into 50 ohms

A/D Converters
- **Sampling Rate:** Up to 250 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
- **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air cooled, Level L3 conduction-cooled, ruggedized

Ordering Information

Model	Description
3312	4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - FMC

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

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