AV 129

S-Band, C-Band and X-Band
Phased-Array Radar Transceiver
MIMO

3U VPX
Kintex UltraScale FPGA
Quad 14 bit 3 Gsps ADC – Quad 16 bit 6 Gsps DAC
Conduction or Air-Cooled

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV129

Applications

- Radar S-Band, C-Band and X-Band Transceiver
- MIMO

Features

- 4 channels 3 Gsps 14-bit ADC
- independent Digital Down Converters, decimation factor 2 to 48.
- 4 channels 6/12 Gsps 16-bit DAC
- independent Digital Up Converters, interpolation 2 to 24.
- One Ultra Low jitter clock synthesizers
- External or internal sampling clock
- External and internal sampling clock reference
- User programmable Xilinx® Kintex® Ultrascale™ KU115 FPGA
- 800 MHz 2x 256M64 DDR3 SDRAM
- 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions

Overview

The AV129 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.
The AV129 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.
The AV129 combines four 14-bit 3 Gsps ADCs and four 16-bit 6/12 Gsps DAC with ultra-high processing power delivered by Xilinx® Kintex® Ultrascale™ FPGA, making it ideally suited for fully synchronous multiple channels test and measurement, MIMO, Electronic Warfare or Ultra-Wideband Radar Transceiver applications.
The AV129 features an internal ultra-low jitter reference and one clock synthesizers and can be used with either external clock or external reference for higher flexibility.
The AV129 includes one Xilinx® Kintex® Ultrascale™ KU115 FPGA for an impressive processing capability of more than 7 TMACs (Multiply Accumulate per second), two high speed 256M64 DDR3 SDRAM memory for data processing and two 1 Gb synchronous FLASH memory for multiple firmware storage.
The AV129 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.
The AV129 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

14-bit 3 Gsps ADC

The AV129 Analog to Digital conversion is performed by two Analog Devices AD9208 14-bit 3 Gsps ADCs with independent Digital Down Converters with decimation factor ranging from 2 to 48 in complex mode.
The AV129 provides four front panel SMPM connectors for analog inputs.
Single ended input signals are AC coupled with a full power input bandwidth from 2 GHz to 8 GHz with 6 dBm input level and up to X-Band with higher input level
A wideband signal generator is provided for on board, stand-alone calibration.

16-bit 6/12 Gsps DAC

The AV129 Digital to Analog conversion is performed by four Analog Devices AD9162 16-bit 6/12 Gsps DACs with independent Digital Up Converters with interpolation factor ranging from 2 to 24 in complex mode.
The AV129 provides four front panel SMPM connectors for analog outputs.
Single ended output signals are AC coupled with an output bandwidth from 2 GHz to 7.5 GHz with 0 dBm output level. X-Band signals are supported with lower signal level.

Clock

The AV129 provides one ultra-low jitter clock synthesizers locked on a 100 MHz internal reference. The AV129 supports a 10 to 100 MHz external reference input either froma front panel SMPM connector or from the VPX P2 Connector.
External clock inputs for the ADCs are supported from either one SMPM connector or VPX P2.
External clock from 2 GHz to 6 GHz are supported.

FPGA

The AV129 is fitted with a Xilinx® Kintex® Ultrascale™ KU115 user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring sub-system, leaving most of the logic and block RAM and all DSP resources available for customer processing.
Dedicated to signal processing, the Xilinx Kintex Ultrascale KU115 FPGA includes 1,451 K logics cells, 2,160 36 Kbit RAM blocs, 6 PCIe interface blocs and 5,520 DSP48 slices for an impressive processing power of more than 7 TMACs.
The FPGA is delivered in -2 speed grade.

Memories

The AV129 includes two 800 MHz 256M64 DDR3 SDRAM memory banks and two 1 Gbit QSPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV129 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV129 also supports 28 single ended LVCMOS33 plus 8 single ended LVCMOS18 on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.
The AV129 features two low phase noise clock generators able to synthesize clock references for the FPGA GTHs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 12.5 Gbps.

Microcontroller

The AV129 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.
The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.
The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware

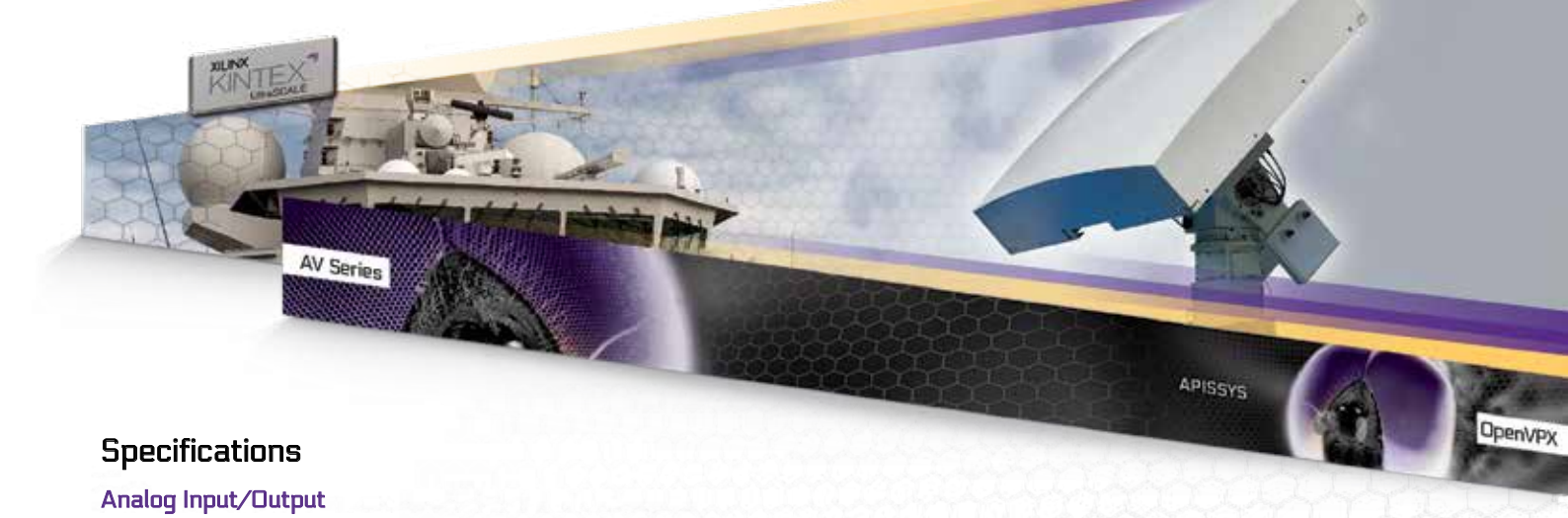
The AV129 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV129 hardware resources.
A base design is provided which demonstrates the use of the AV129 and gives users a starting point for firmware development. The AV129 firmware package is supported on the Xilinx VIVADO® 2016.4 design suite and later.

Software

The AV129 is delivered with software drivers for Windows 10 and Linux.

Ruggedization

The AV129 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC_4, EAC_6, ECC_3 and ECC_4.



Specifications

Analog Input/Output

- Input coupling: AC
- Full power bandwidth: 2 to 8 GHz
- Full scale : 6 dBm
- Output coupling: AC
- Full power bandwidth: 2 to 7.5 GHz
- Full scale : 0 dBm
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion

- Four channels, Fs ≤ 3 GHz
- Resolution: 14 bit
- Sampling Performances @2.6 GHz -2dBFS
- SNR: 57 dBFS
- SFDR: 70 dBc
- ENOB: 9.0 bit

Digital-Analog Conversion

- Four channels, Fs ≤ 6 GHz
  (12 GHz DAC update rate)
- Resolution: 16 bit
- Sampling Performances @2 GHz 5 Gsps
  - SFDR: 70 dBc (0dBFS)
  - NSD: -155 dBm/Hzt

Clock

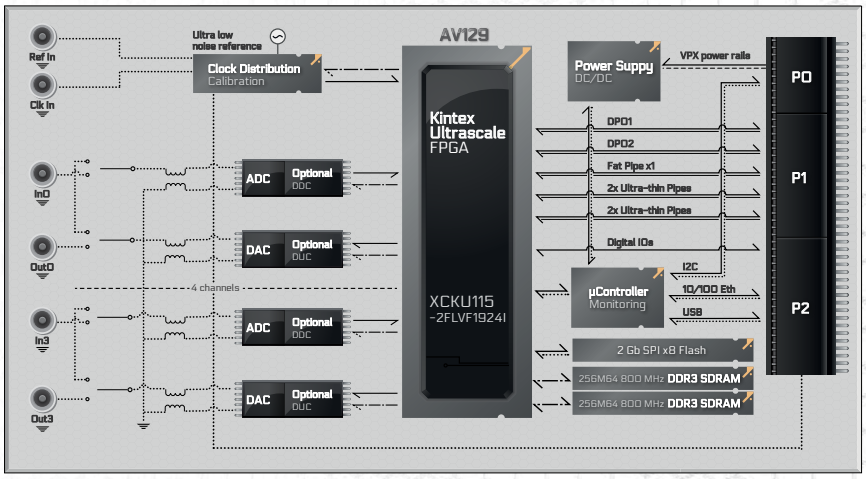
- Internal:
  - One ultra-low jitter clock synthesizers,
  - 2 GHz to 6 GHz low jitter clock
- External Input Clock:
  - Frequency: 2 GHz to 6 GHz
  - Input level: 10 dBm recommended
  - Connector: SMPM 50 Ohms and VPX P2
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

Digital Down Converterr

- 2 independent DDC for each ADC:
  - Tuning frequency step: 48-bit NCO
  - DDC with 1/2 to 1/48 decimation ratio with I-Q complex output.

Digital Up Converter

- 1 DUC for each DAC:
  - Tuning frequency step: 48-bit NCO
  - DUC with 1/2 to 1/24 interpolation ratio



FPGA

- FPGA: Xilinx Kintex Ultrascale
  - XCKU115-2FLVF1924

Memory

- Two banks 256M64 DDR3 SDRAM, 800 MHz clock
- Two 1 Gbit QSPI FLASH memory

VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 28 single ended LVCMOS33
  - 8 single ended LVCMOS18

Software support

- Software Drivers:
  - Windows 10
  - Linux
- Application example: Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2016.4 and later

Ruggedization

- As per VITA 47:
  - Air cooled : EAC_4 and EAC6
  - Conduction cooled : ECC_3 and ECC_4

Power dissipation (KU115)

- +12V: 6.7 A max (80W)
- +5V: 9.0 A max (45W)
- +3.3V: 2.1 A max (7W)
- +3.3VAUX: 0.6 A max (2W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ordering information

Part Number		AV129	-	rr	-	a
Ruggedization level	Air Standard	-	-	AS	-	-
	Air Rugged	-	-	AR	-	-
	Conduction Standard	-	-	CS	-	-
	Conduction Rugged	-	-	CR	-	-
Options 1	FPGA Kintex Ultrascale KU115	-	-	-	-	1

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

Reference to ANSI-VITA standard 47 for the listed parameters only.

www.apissys.com

ApisSys
Archamps Technopole
60 rue Douglas Engelbart
Bâtiment ABC1 entrée A
74160 Archamps, France
Phone: +33 4 50 36 07 58
Fax: +33 4 50 36 05 29